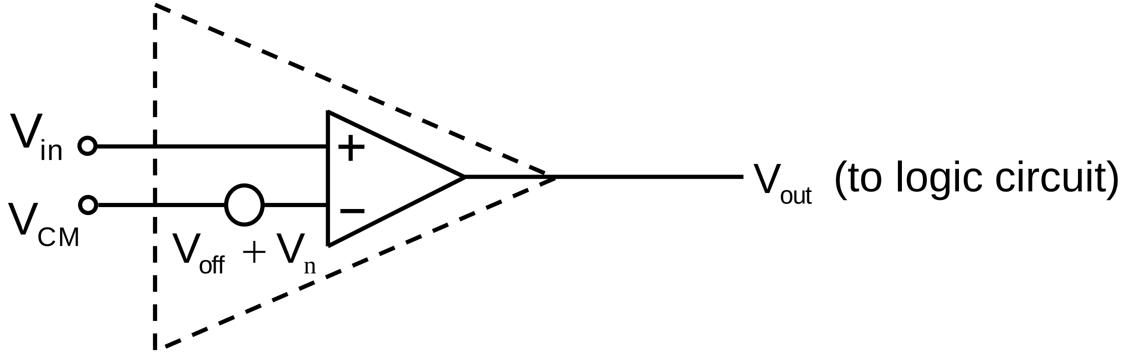
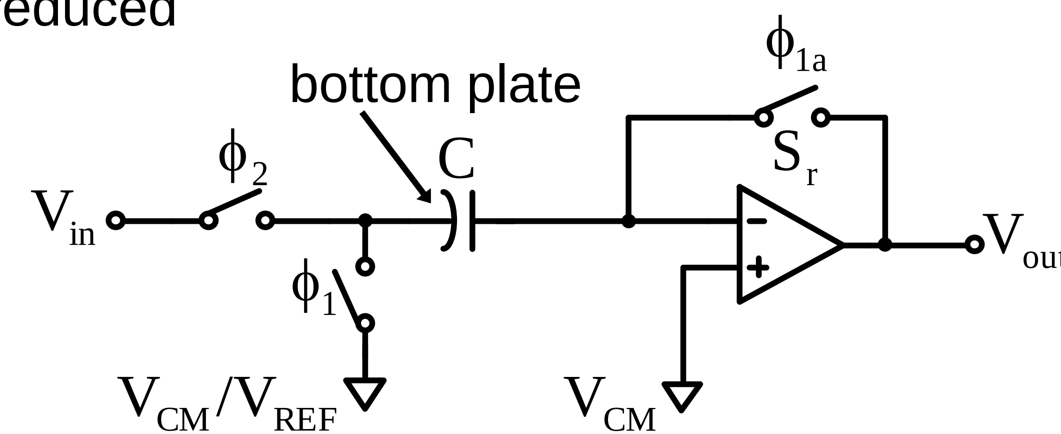
Comparators

Use An OPAMP as A Comparator

- Use for signal levels comparison to generate an output with a digital level

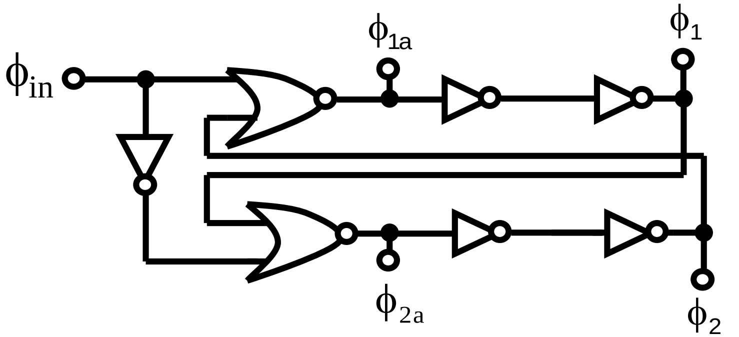


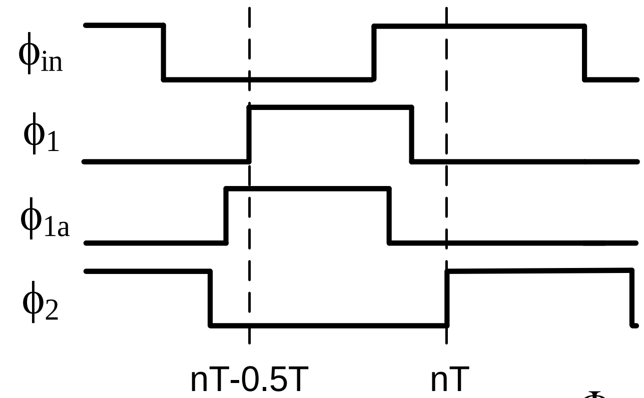
- Disadvantage
  - Slow response: Settle too slowly for large voltage output
  - Limited resolution: Due to input offset voltage
- Offset cancellation: ϕ_{1a} is a slightly advanced version of ϕ_1 so that charge-injection effects are reduced



Use An OPAMP as A Comparator (Cont.)

- ϕ_1 and ϕ_2 are non-overlapped clocks



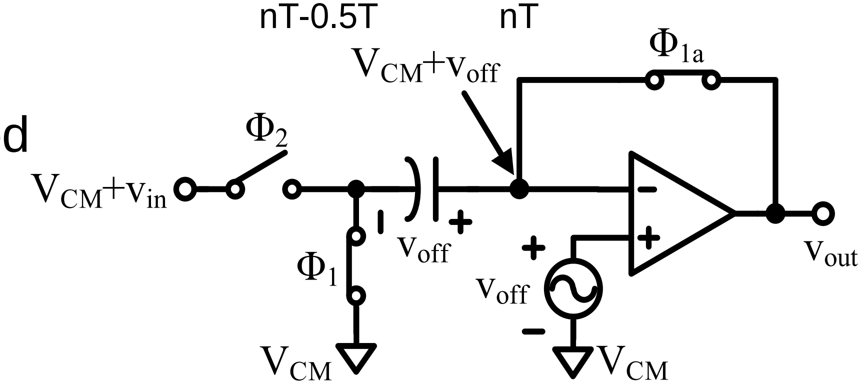


- Reset phase: ϕ_1 high, ϕ_2 low

  Stable OPAMP compensation required

  During ϕ_1 = High (t = nT–T/2)

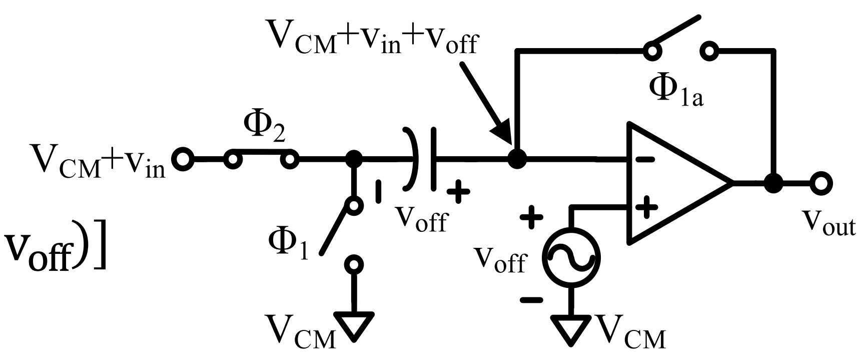
$$v_{out} = V_{CM} + v_{off}$$



- Comparison phase

  During ϕ_2 = High (t = nT)

$$v_{out} = -A[(V_{CM} + v_{in} + v_{off}) - (V_{CM} + v_{off})]$$
$$= -Av_{in}$$



Use An OPAMP as A Comparator (Cont.)

- If OPAMP noise is considered, then v_{off} should be replaced by $v_{off} + v_n$ (ignore the V_{CM} noise)
  - $v_{out}(nT) = -A[v_{in}(nT)+v_n(nT-T/2) - v_n(nT)]$
  - $v_{out}(z) = -A[v_{in}(z)-v_n(z)(1-z^{-0.5})]$ (Correlated Double Sampling, CDS)

$V(nT)$ i.e. $V(n)$

$V(nT-\frac{T}{2})$ i.e. $V(n-\frac{1}{2})$

$V(nT-T)$ i.e. $V(n-1)$

$z = e^{j\omega T}$; $\omega = 2\pi f$

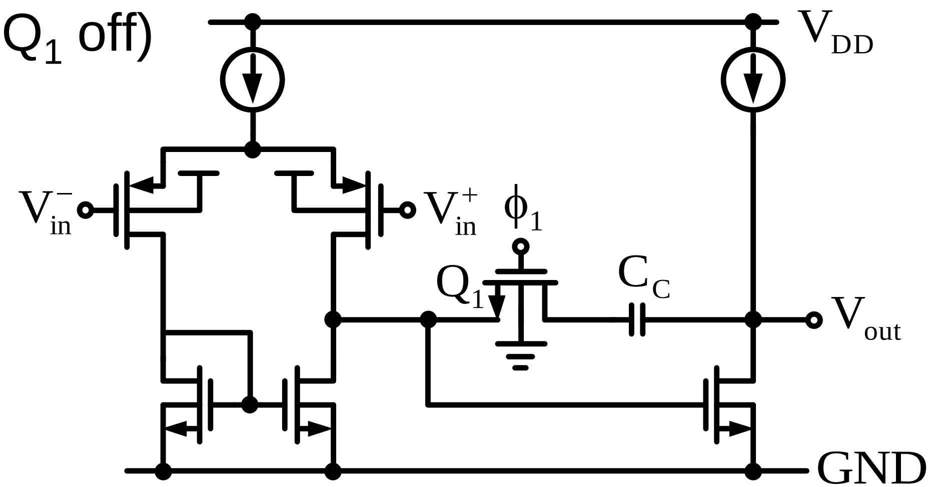
clock signal

$V(n) \longrightarrow V(z)$

$V(n-\frac{1}{2}) \longrightarrow z^{-\frac{1}{2}}V(z)$

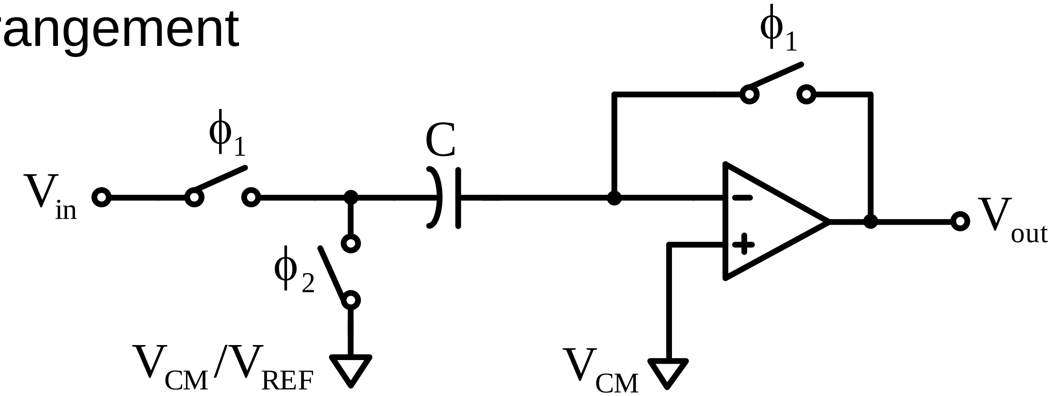
$V(n-1) \longrightarrow z^{-1}V(z)$

- Speed up comparison time
  - Compensation capacitor can be disconnected (by turning Q_1 off)

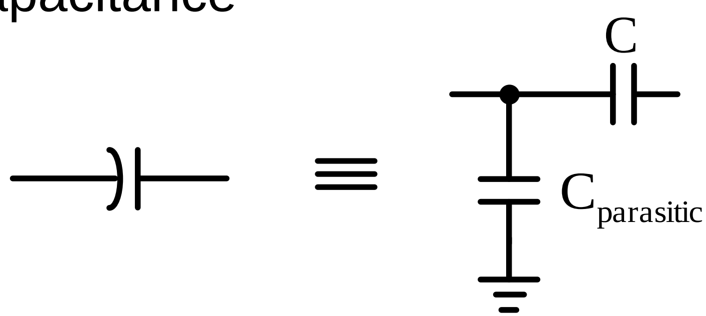


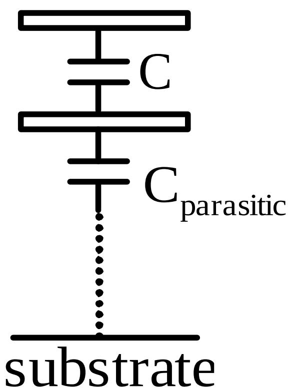
Use An OPAMP as A Comparator (Cont.)

- No need for V_{in} to charge C in the example above
- Poor clock arrangement



  - ◆ V_{in} needs to charge C during ϕ_1 is high
- Parasitic capacitance





  - ◆ V_{in} needs to charge $C_{parasitic}$

Correlated Double Sampling (CDS)

- Offset cancellation technique not only eliminates input offset voltage but also minimizes errors caused by 1/f noise
  - Recall that

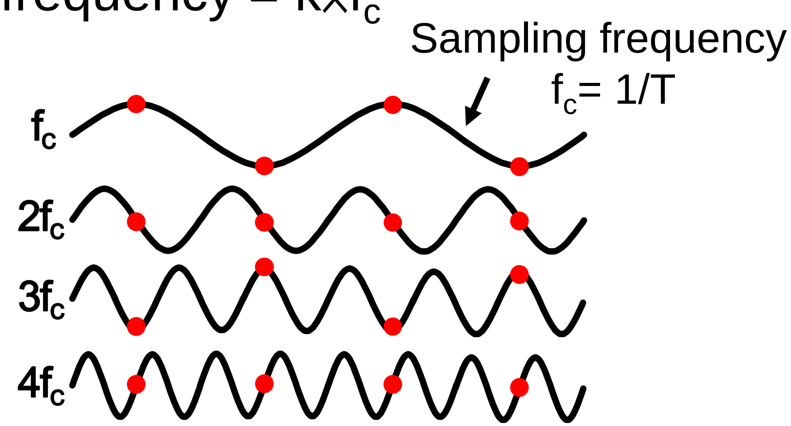
$$V_{out}(z) = -A[V_{in}(z) - V_n(z)(1 - z^{-0.5})]$$

$$\text{Let } H_{CDS}(z) = 1 - z^{-0.5}$$

$$\xrightarrow{z=e^{j\omega T}} H_{CDS}(z) = 1 - e^{\frac{-j\omega T}{2}} = e^{\frac{-j\omega T}{4}} \cdot 2j\sin(\frac{\omega T}{4}) \quad (e^{j\omega T}=\cos(\omega T)+j\sin(\omega T))$$

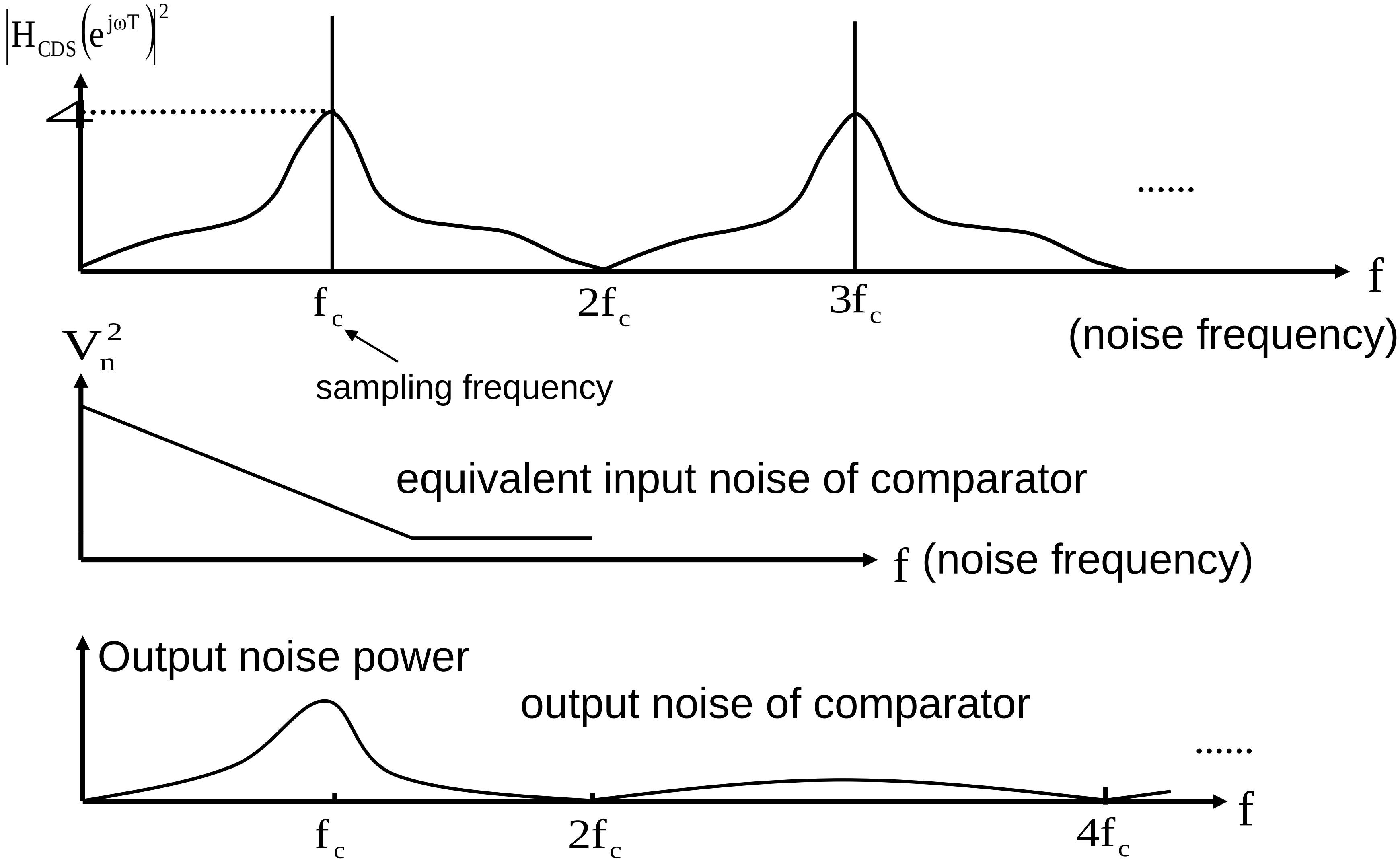
$$\left|H_{CDS}(e^{j\omega T})\right|^2 = 4\sin^2(\frac{\omega T}{4})$$

  - From time domain waveform, if noise frequency = $k \times f_c$
    - When k is an odd number, noise cannot be canceled
    - When k is an even number, noise can be fully canceled



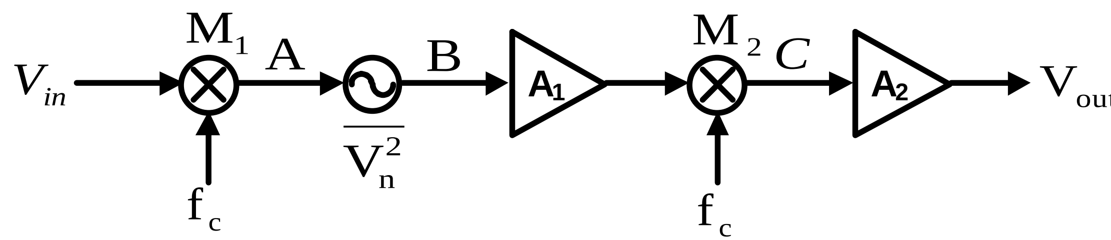
Correlated Double Sampling (CDS)

- Noise shaping function $H_{CDS}(e^{j\omega T})$

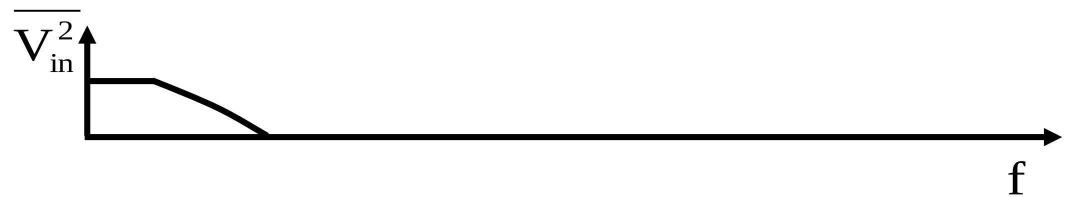


Chopper-Stabilized Amplifier

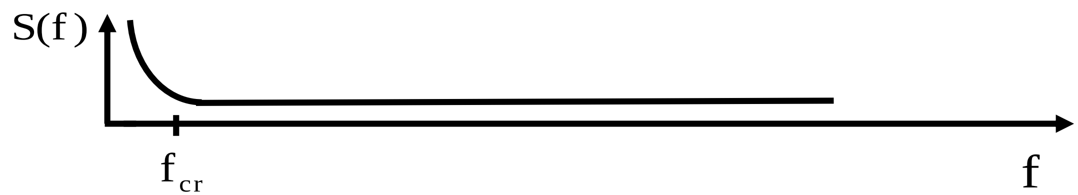
- Can also be used to reduce 1/f noise
- Basic concept
  - ◆ Block diagram



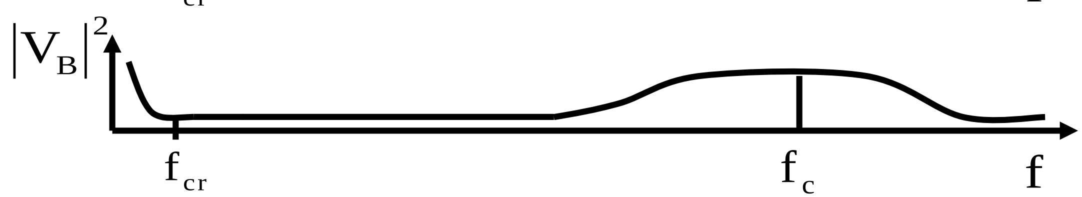
  - ◆ Input spectrum



  - ◆ Noise spectrum



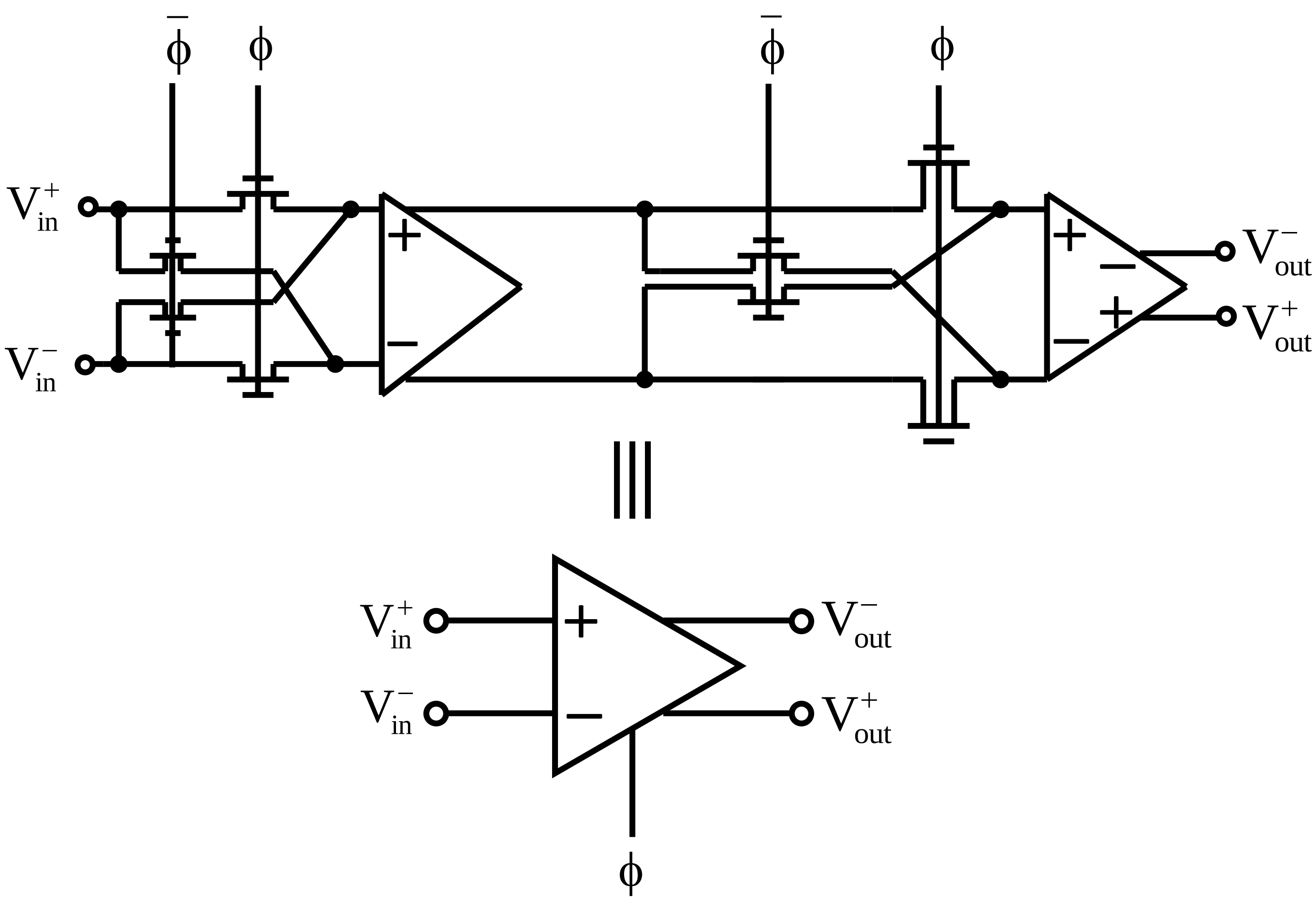
  - ◆ The spectrum at node B



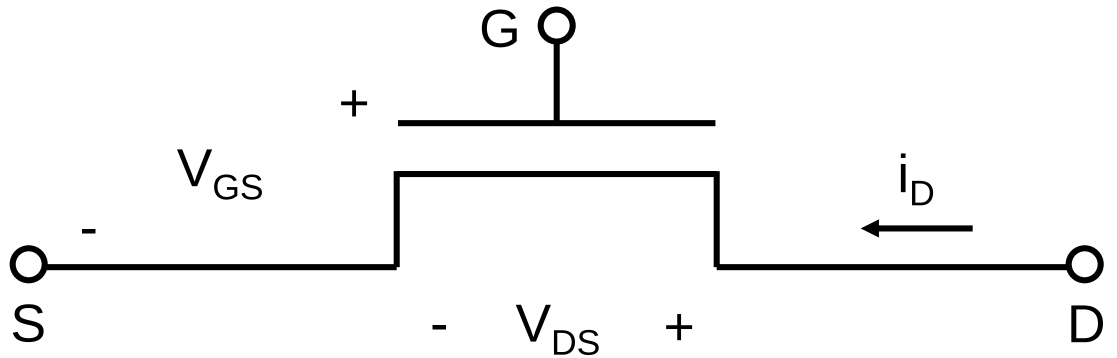
  - ◆ The spectrum at node C

Chopper-Stabilized Amplifier (Cont.)

- Implementation example
  - A differential chopper-stabilized OPAMP



MOS Switches



- Usual Case： $|V_{GS} - V_T| \gg |V_{DS}| \Rightarrow i = \mu C_{ox}\frac{W}{L}[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2]$
- MOSFET behaves like a linear resistor of value

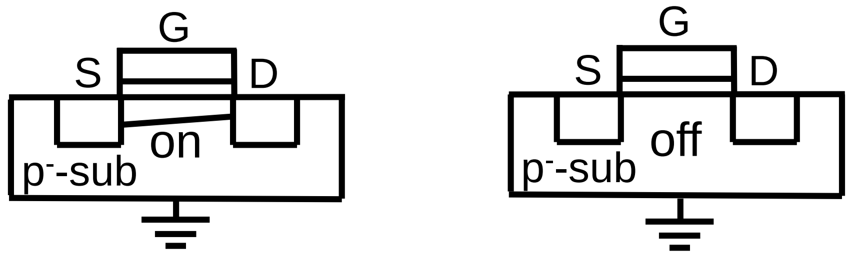
$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)}$$

- Gate - control terminal
- Drain - input/output
- Source - input/output

} could be exchanged

MOS Switches

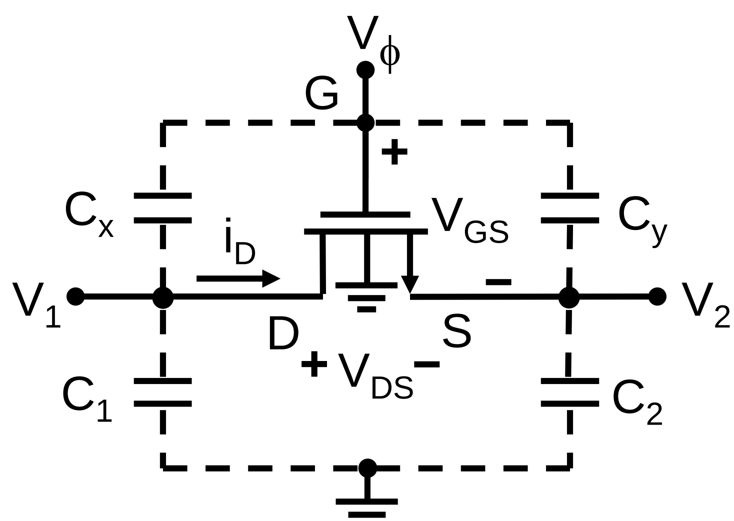
- Channel charge redistribution
  - When switch is turned off, the channel charge is swept in part into drain and in part into source.



- Clock feedthrough

$$\Delta V_1 = \frac{C_x}{C_1 + C_x}\Delta V_\phi$$

$$\Delta V_2 = \frac{C_y}{C_2 + C_y}\Delta V_\phi$$

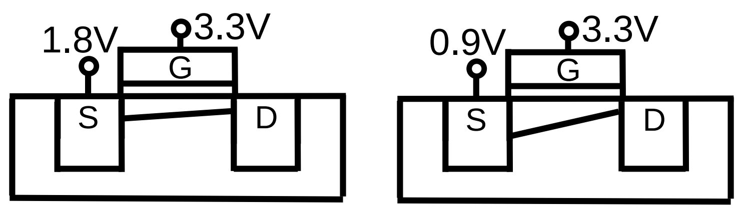


Charge-Injection Errors

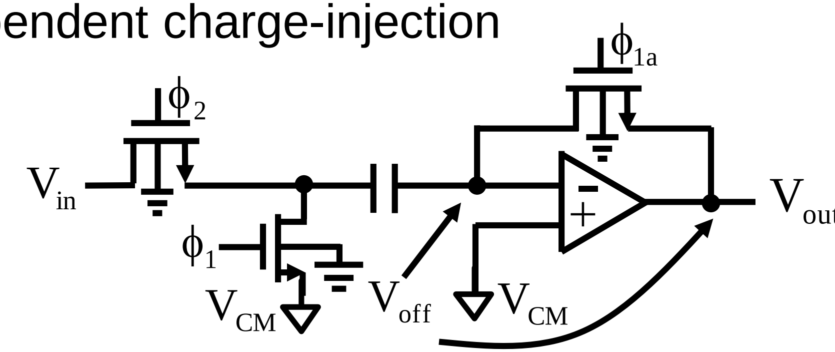
- Two major sources
  - ◆ Channel charge of a transistor with V_{DS}=0

    $Q_{CH} = WLC_{ox}V_{eff} = WLC_{ox}(V_{GS} - V_{th}) = C_gV_{eff}$
    - ➢ MOS switches off ➔ Q_{CH} flows from channel to drain & source junctions
    - ➢ For n-channel MOSFETs, channel charge is negative
  - ◆ Clock feedthrough due to overlap capacitance C_{gs} or C_{gd}

  (Channel charge injection dominates)
- Signal dependent charge-injection
  - ◆ Example

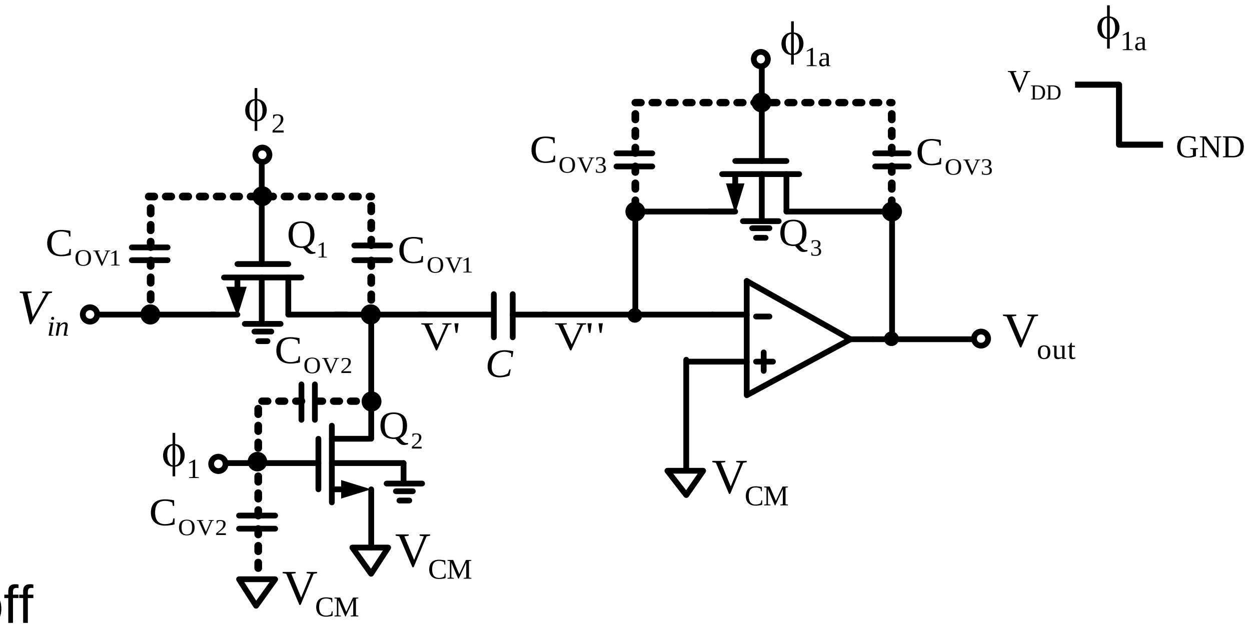


- Signal independent charge-injection



Charge-Injection Errors (Cont.)

- Example



- When Q_3 turns off
  - Voltage change due to channel charge - - - - - - - - - - - - (1)

$$\Delta V'' = \frac{(Q_{CH}/2)}{C} = -\frac{V_{eff} C_{ox} W_3 L_3}{2C} = -\frac{(V_{DD} - V_{CM} - V_{tn}) C_{ox} W_3 L_3}{2C}$$

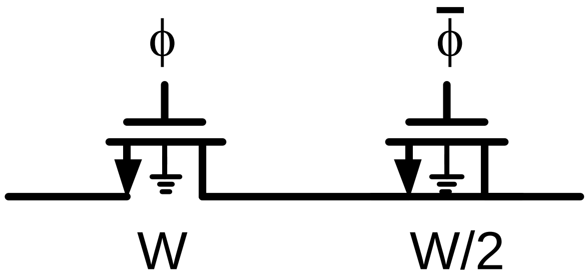
  - Voltage change due to clock feedthrough - - - - - - - - - - (2)

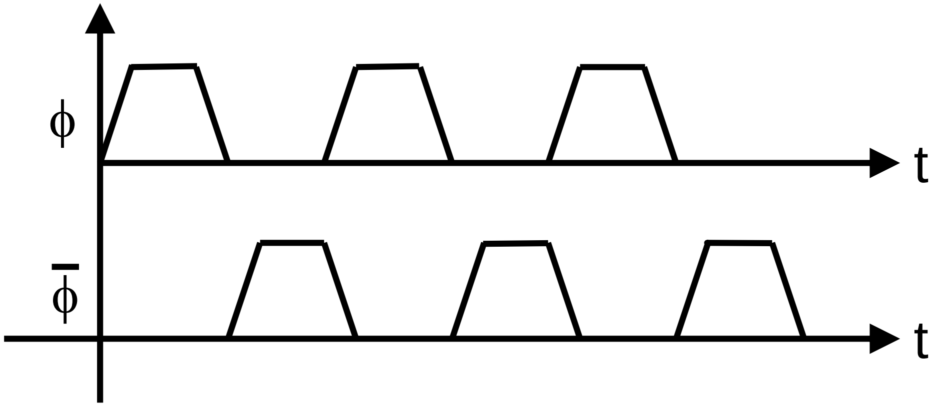
$$\Delta V'' = -\frac{(V_{DD} - GND) C_{ov3}}{C_{ov3} + C}$$

(2) is normally less than (1)

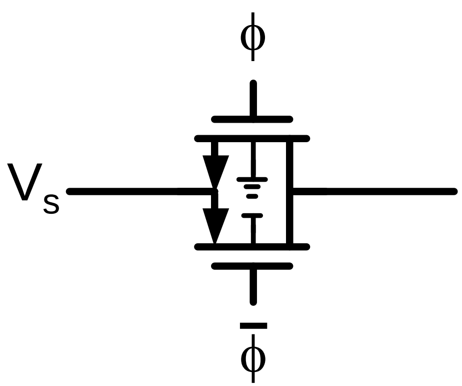
Clock Feedthrough Charge-Injection Compensation

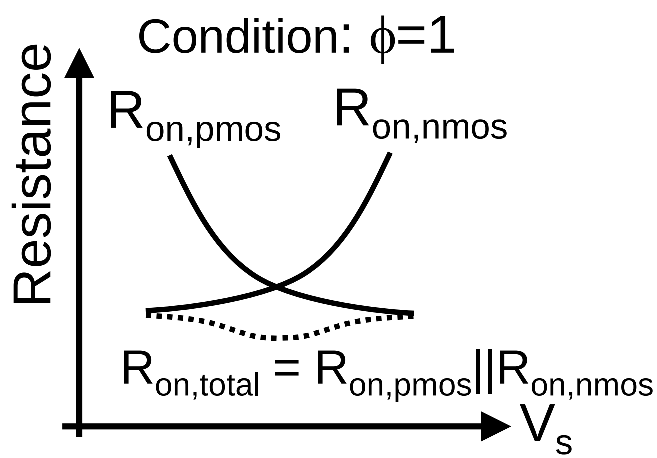
- Method-1：





- Method-2：
  - Uses CMOS transmission gate

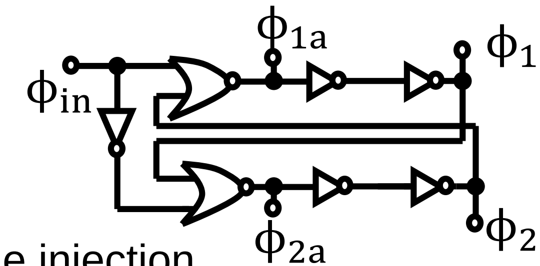


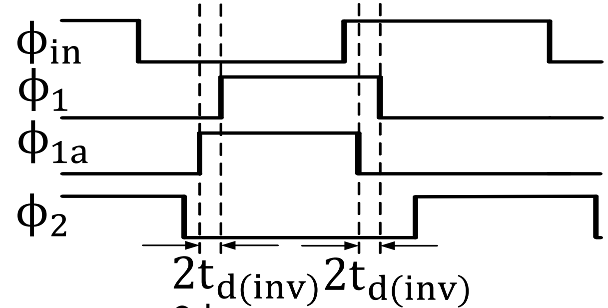


- However, the distribution of the charge is unpredictable, this make perfect clock feedthrough compensation very difficult with any scheme.

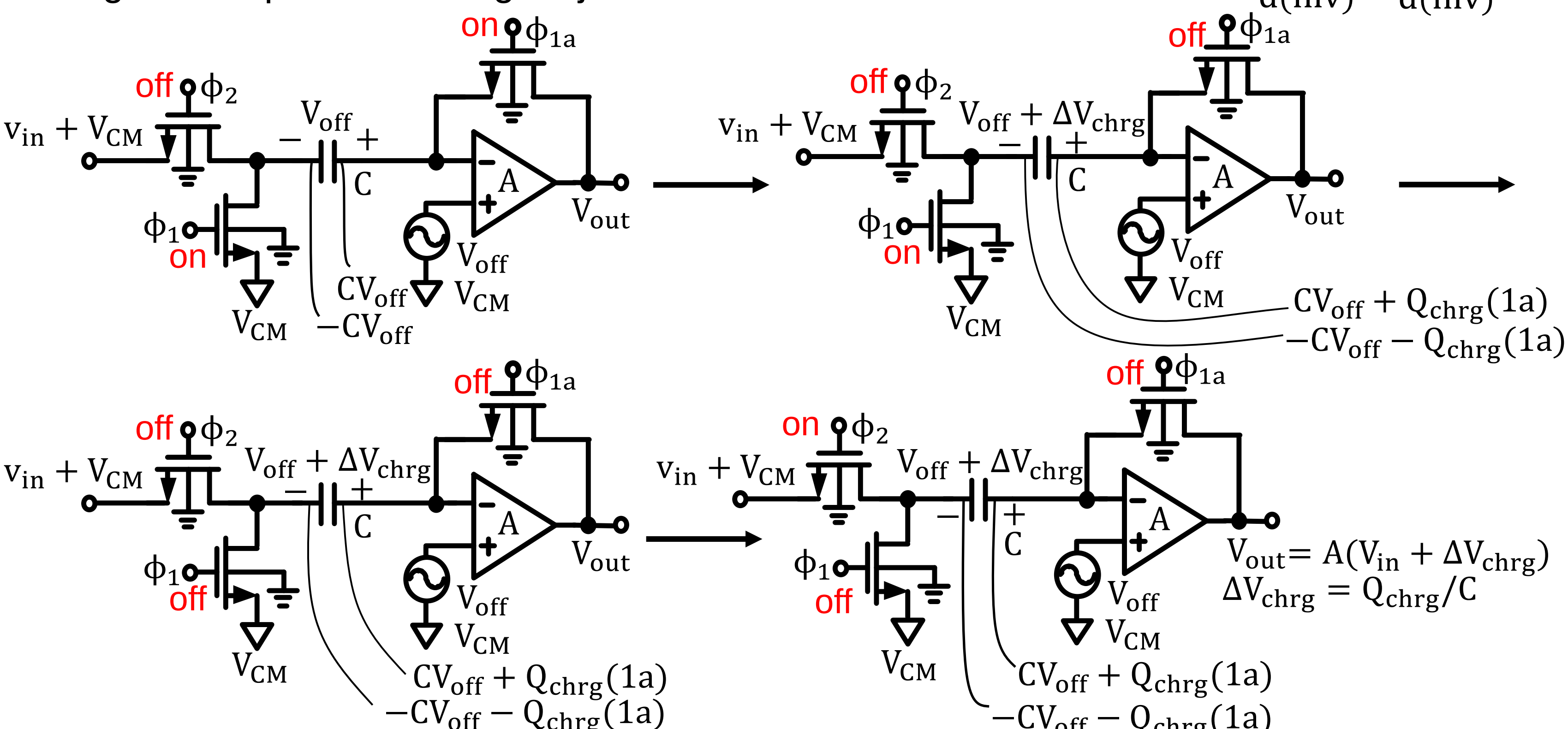
Making Charge-Injection Signal Independent

- Nonoverlapped clocks





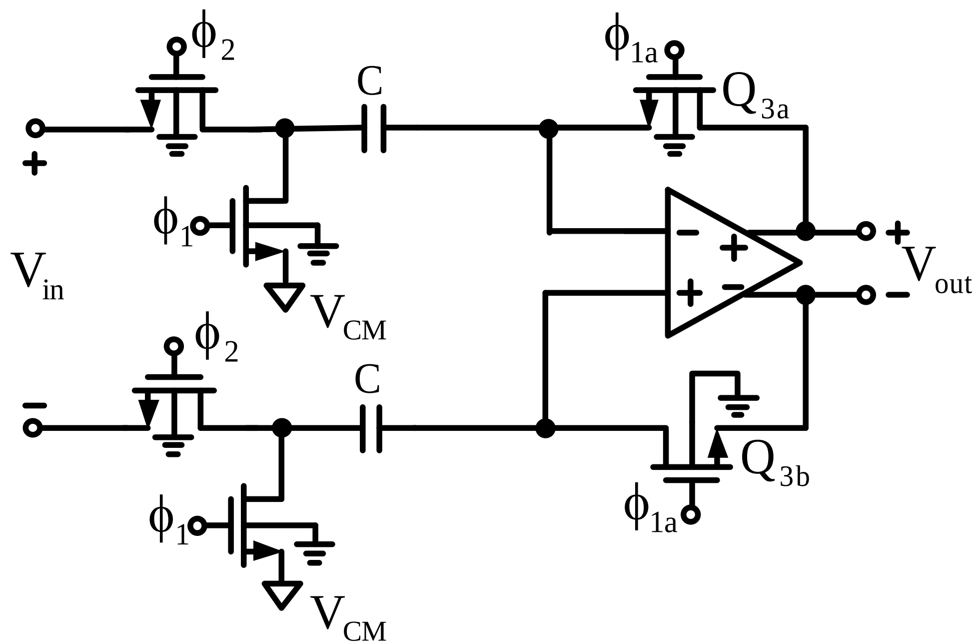
- Signal-independent charge injection



- Constant charge-injection error can be treated as a DC signal and thus can be ignored in most signal processing applications.

Minimizing Errors Due to Charge-Injection

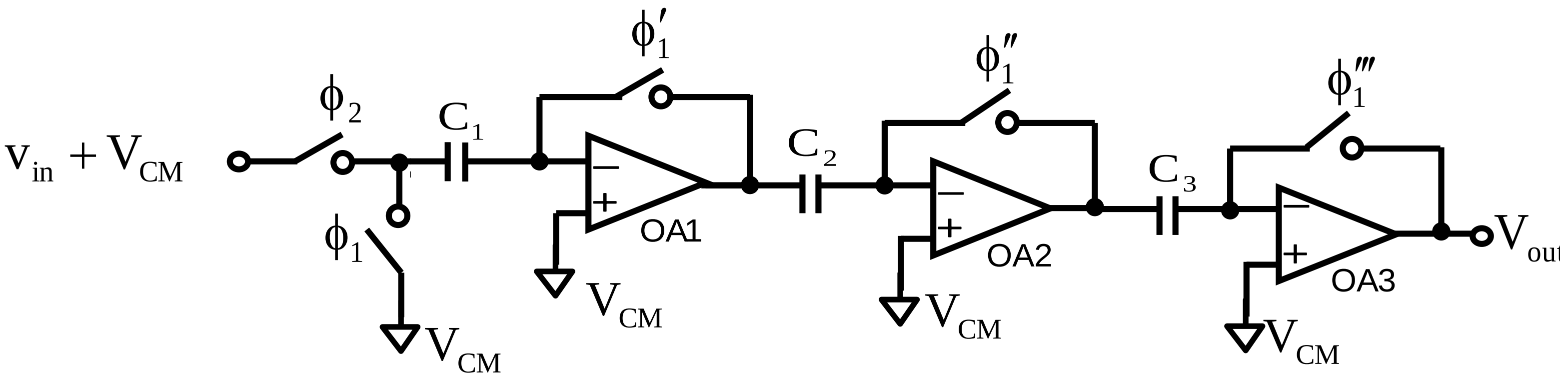
- Use larger C
  - Large silicon area
  - Large parasitic capacitance(Typically, ~20%C)
  - Large power consumption
- Use fully differential design
  - Errors will typically be at least ten times smaller than in the single-ended case

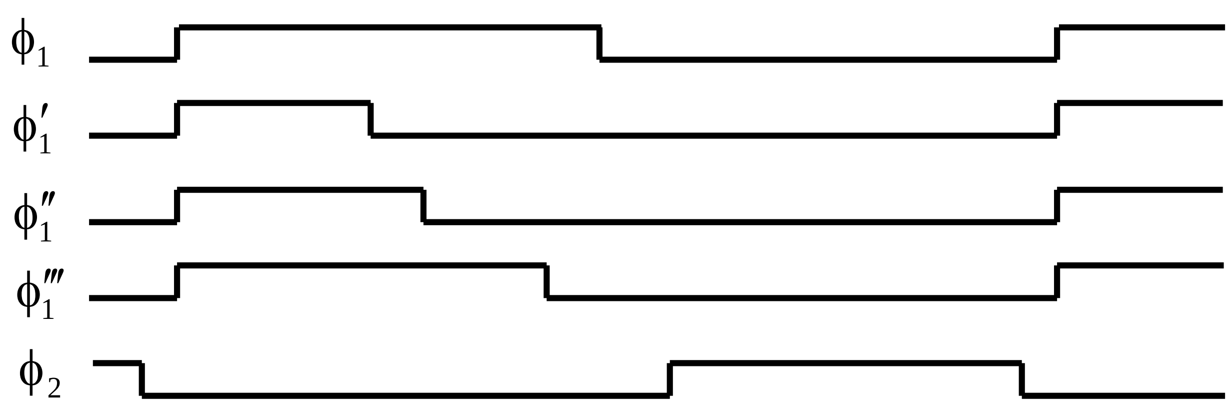


Minimizing Errors Due to Charge-Injection (Cont.)

- Realize a multi-stage differential comparator

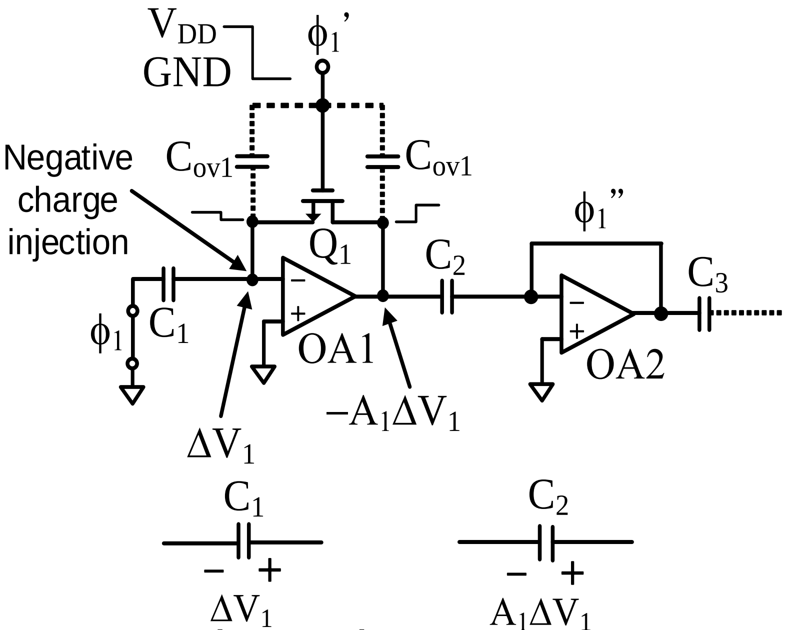
  (For simplicity, single-ended case is used for explanation)
  - Very-high resolution comparator
  - Multi-phase clocks, which slow down the circuit



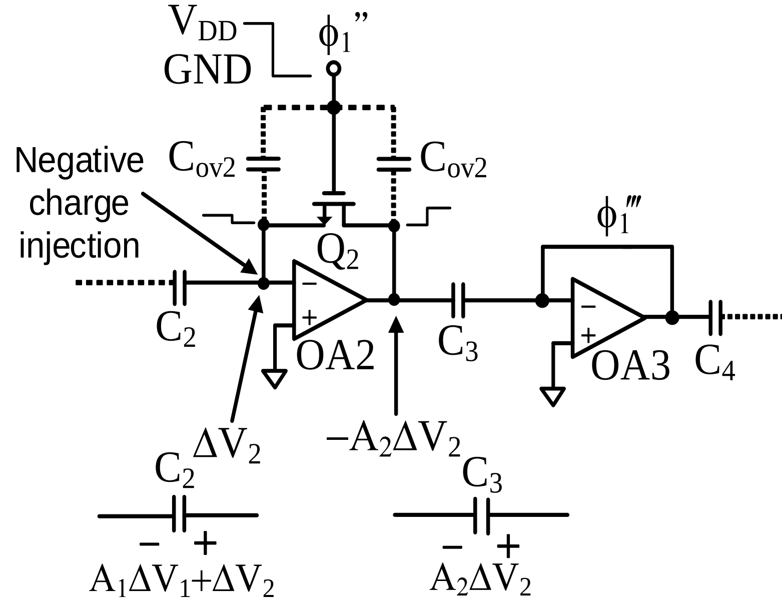


Minimizing Errors Due to Charge-Injection (Cont.)

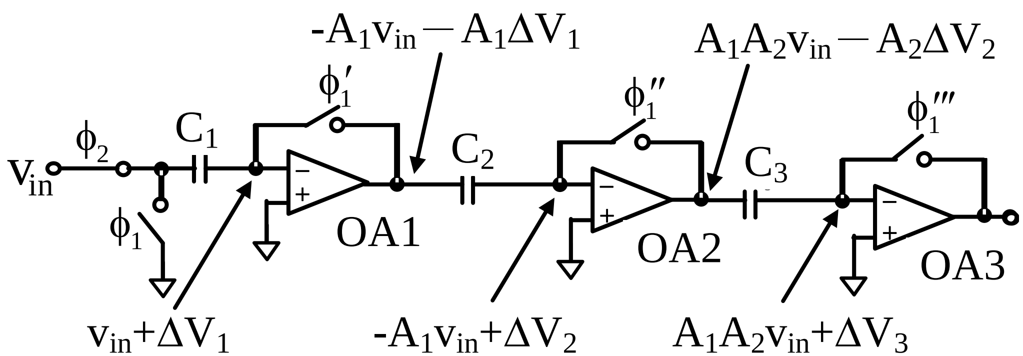
- When ϕ_1' turns off



- When ϕ_1'' turns off



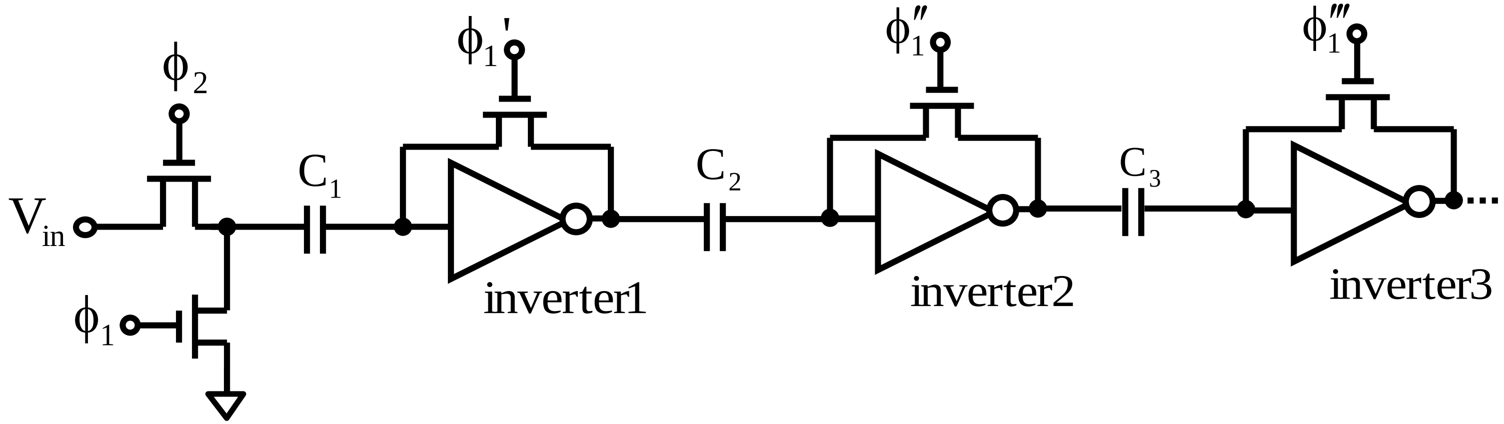
- Comparison phase

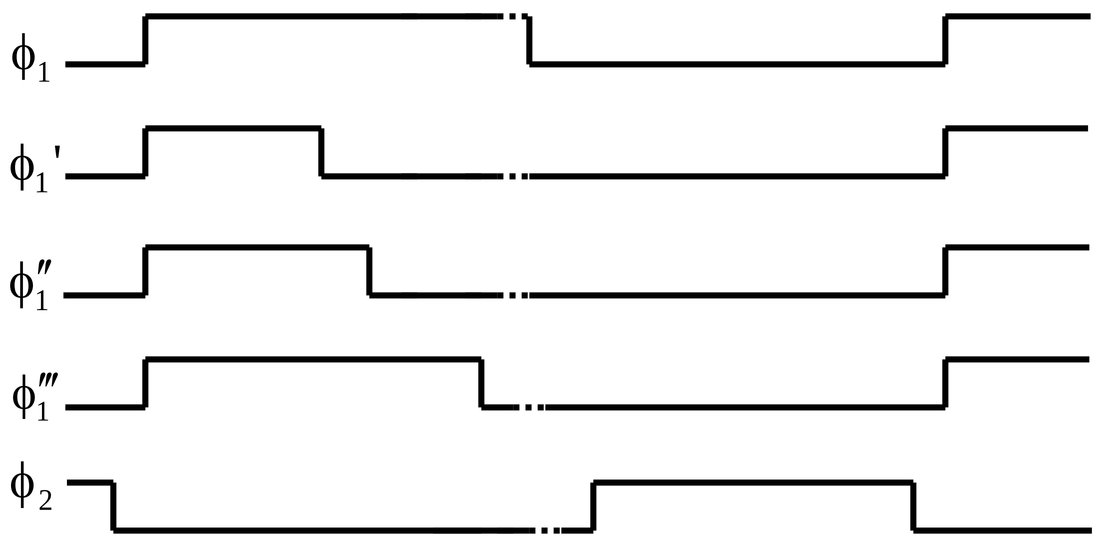


$V_{out} = -A_1A_2A_3v_{in} - A_3\Delta V_3$

Minimizing Errors Due to Charge-Injection (Cont.)

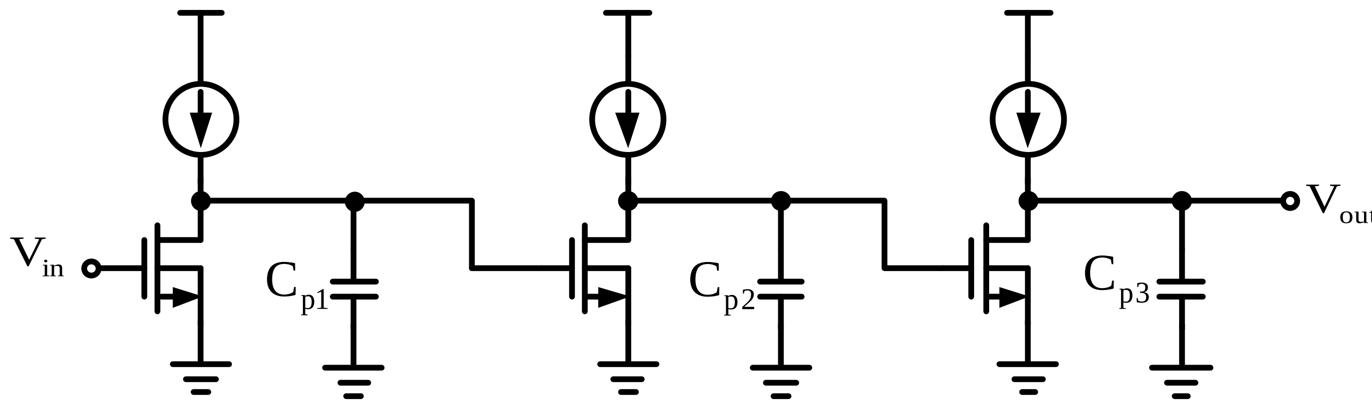
- A high-speed multi-stage comparator using inverters





Speed of Multi-Stage Comparators

- Typically, each stage consists of a single-stage amplifier that has only a 90^0 phase shift and therefore does not need compensation capacitors.



- The parasitic load capacitance at the output of the i^{th} stage is approximately given by $C_{pi} \cong C_{0\text{-}i} + C_{gs\text{-}i+1}$

  where $C_{0\text{-}i}$ is the output capacitance of the i^{th} stage

  $C_{gs\text{-}i+1}$ is the gate-source capacitance of the input transistor of the succeeding stage

  - Normally $C_{0\text{-}i} < C_{gs\text{-}i+1} \Rightarrow C_{pi} < 2C_{gs\text{-}i}$

    Taking $C_{pi}=2C_{gs\text{-}i}$ (as a worst case)

Speed of Multi-Stage Comparators (Cont.)

- The transfer function of a single stage comparator (or amplifier) can be approximated as

$$A_i(s) = \frac{A_{0-i}}{1 + s/\omega_{p-i}}$$

where -3dB frequency

$$\omega_{p-i} \cong \frac{\omega_{t-i}}{A_{0-i}} \approx \frac{1}{A_{0-i}} \frac{g_{mi}}{2C_{gs-i}}$$, where $\omega_{t\text{-}i}$ is the unit gain frequency

Hence, time constant

$$\tau_i = \frac{1}{\omega_{p-i}} \approx \frac{2A_{0-i}C_{gs-i}}{g_{mi}}$$

- The overall transfer function for a cascaded n-stage comparator

$$A_{total}(s) = \prod_i A_i(s) = \frac{A_{0-1} \cdot A_{0-2} \ldots A_{0-n}}{\left(1 + \frac{s}{\omega_{p-1}}\right)\left(1 + \frac{s}{\omega_{p-2}}\right) \ldots (1 + \frac{s}{\omega_{p-n}})}$$

Speed of Multi-Stage Comparators (Cont.)

Ignoring higher-order terms results in

$$A_{total}(s) = \frac{\prod A_{0-i}}{1 + s(\sum_i \frac{1}{\omega_{p-i}})} \cong \frac{A_o^n}{1 + n\left(\frac{s}{\omega_{p-i}}\right)}$$

- Time constant

$$\tau_{total} \cong \frac{2nA_oC_{gs}}{g_m} \cong 2nA_o\tau_T = n\tau_i$$

where $\tau_T = \frac{1}{\omega_T} = \frac{C_{gs}}{g_m}, \tau_i = 2A_0\tau_T$

ω_T is unity-gain frequency of a single amplifier

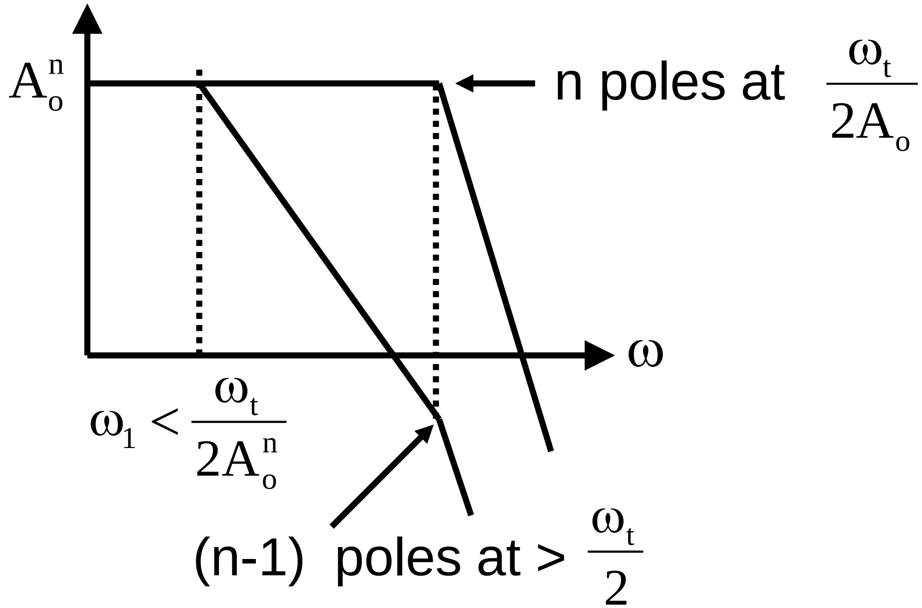
- A single OPAMP with the same gain as the multi-stage comparator

$$A(s) = \frac{A_o^n}{(1+\frac{s}{\omega_1})(1+\frac{s}{\omega_2})^{n-1}} \approx \frac{A_o^n}{1+\frac{s}{\omega_1}}$$

Dominant pole (n-1) nondominant poles

Speed of Multi-Stage Comparators (Cont.)

$$\text{Time constant} > 2A_0^n \tau$$



- ◆ Lower speed compared to multi-stage one

- $C_{gs} = \frac{2}{3} C_{ox} WL$ and $g_m = \mu C_{ox} \frac{W}{L} V_{eff}$

$$\Rightarrow \tau_{total} = \frac{4nA_0L^2}{3\mu_n V_{eff}}$$

Speed of Multi-Stage Comparators (Cont.)

$$\tau_{total} \cong 2nA_0\tau_t = 2n \cdot \sqrt[n]{A_{total}}\,\tau_t \qquad \text{Note}: \frac{\partial A^n}{\partial n} = A^n \ln(A)$$

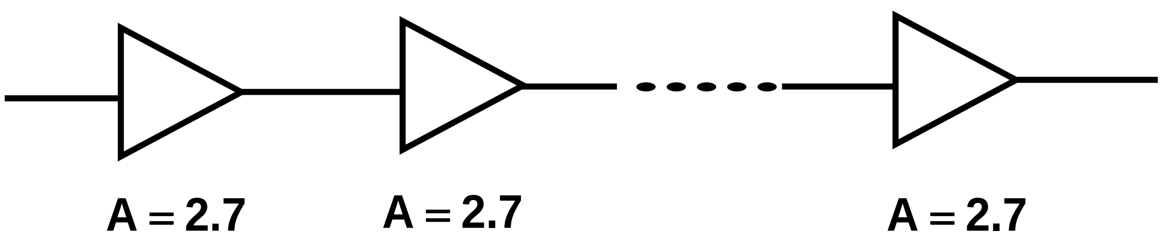
For minimum τ_{total}

$$\frac{\partial \tau_{total}}{\partial n} = 2A_{total}^{1/n}\tau_t + 2n(-\frac{1}{n^2})A_{total}^{1/n}\tau_t \ln(A_{total}) = 0$$

$$\Rightarrow 1 - \frac{1}{n} \cdot \ln(A_{total}) = 0$$

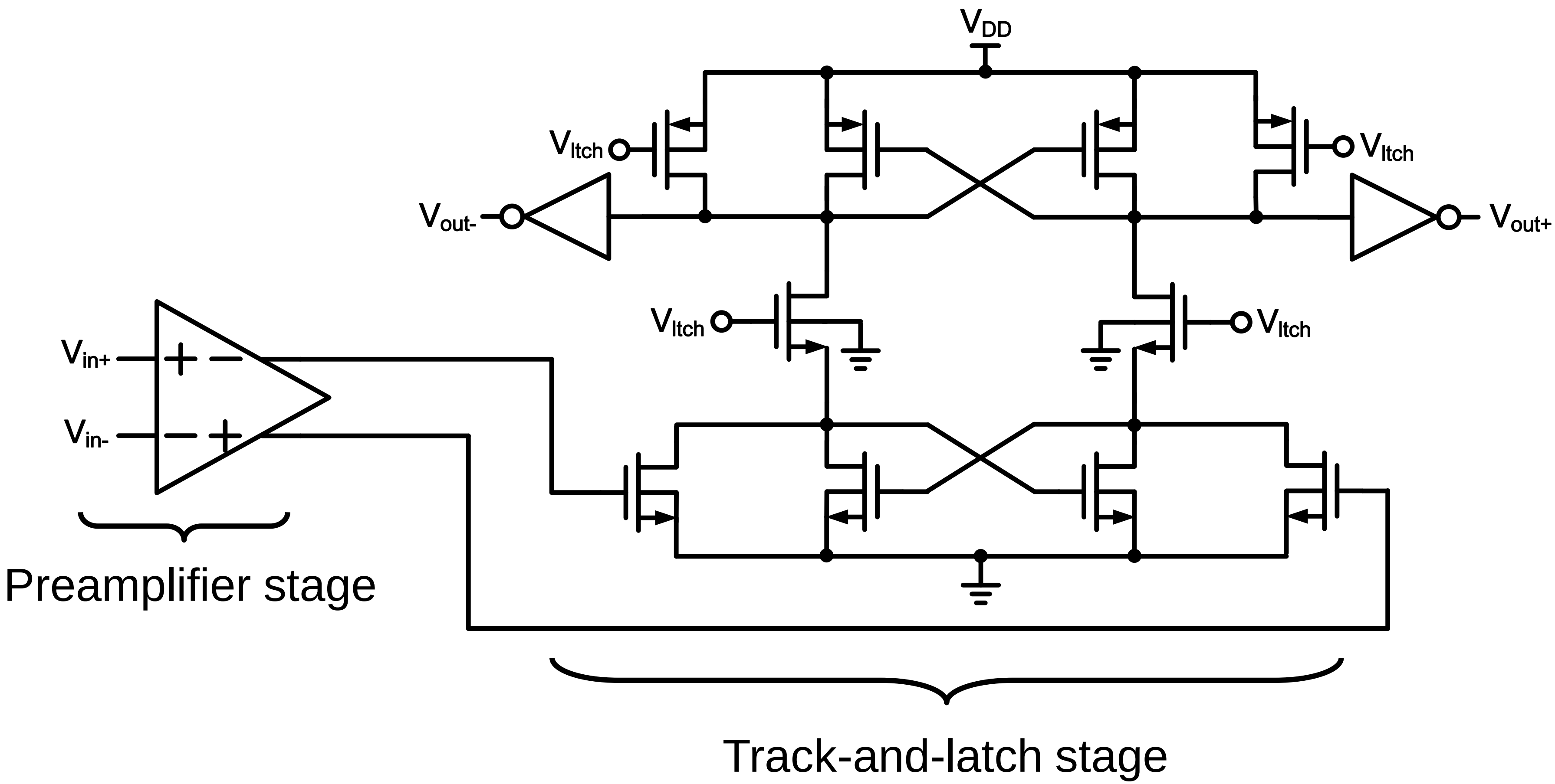
$$\Rightarrow n = \ln(A_{total})$$

$$\Rightarrow A_{total} = e^n$$



Latched Comparators

- Typical design: Preamplifier + track-and-latch stage
  - A CMOS example



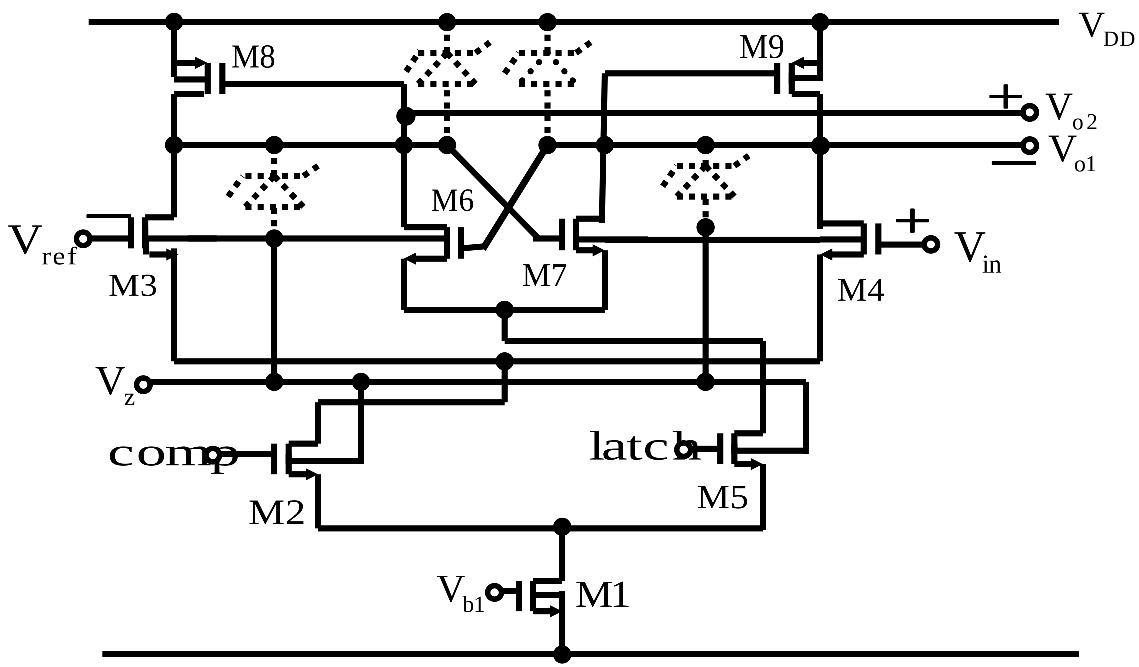
Latched Comparators (Cont.)

- Preamplifier
  - 1 or 2 stages
  - Two purposes
    - To obtain higher resolution
    - To minimize kickback effects

      (kickback denotes the charge transfer either into or out of the inputs when the track-and-hold stage goes from track mode to latch mode)
  - Typical gain : 4~10 $\quad \text{gain} \uparrow \Rightarrow \begin{cases} \text{resolution} \uparrow \\ \text{speed} \downarrow \end{cases}$
  - Without a preamplifier or buffer, the kickback will enter the driving circuitry and cause very large glitches, especially in the case when the impedance seen looking into the two inputs are not perfectly matched.

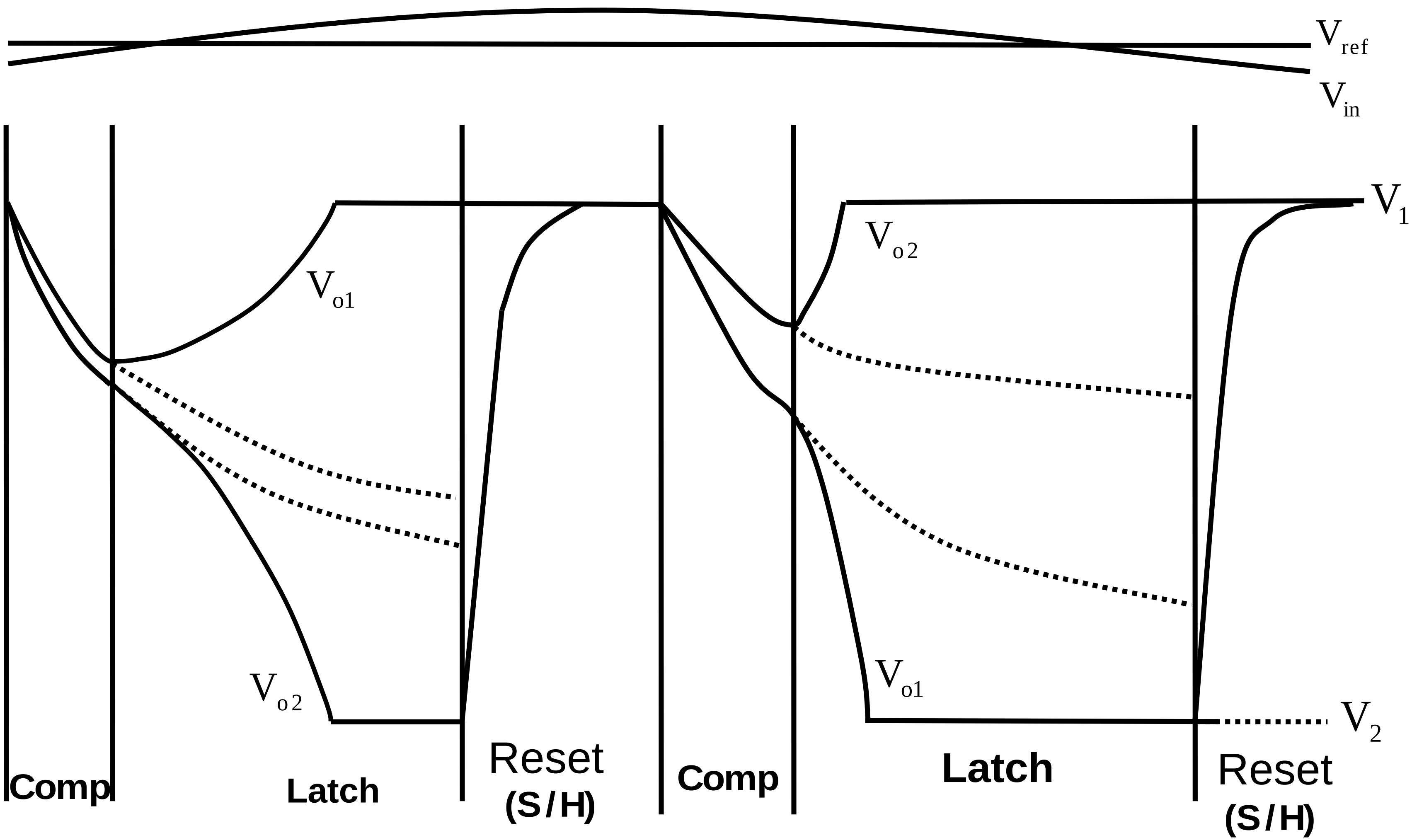
Latched Comparators (Cont.)

- Track-and-latch
  - Amplifies preamplifier output
  - Use positive feedback to generate full-scale digital signal (i.e. Its equivalent gain is infinite during latch phase)
    - Minimizes the total number of gain stages required
    - Faster than the multi-stage approach
  - Example



Latched Comparators (Cont.)

- Comparator output waveform



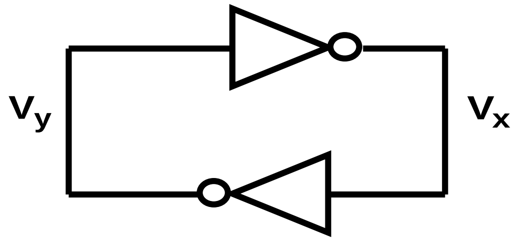
Latched Comparators (Cont.)

- Capacitive coupling and reset switches can be included to eliminate any input-offset-voltage and clock-feedthrough errors, as described before.

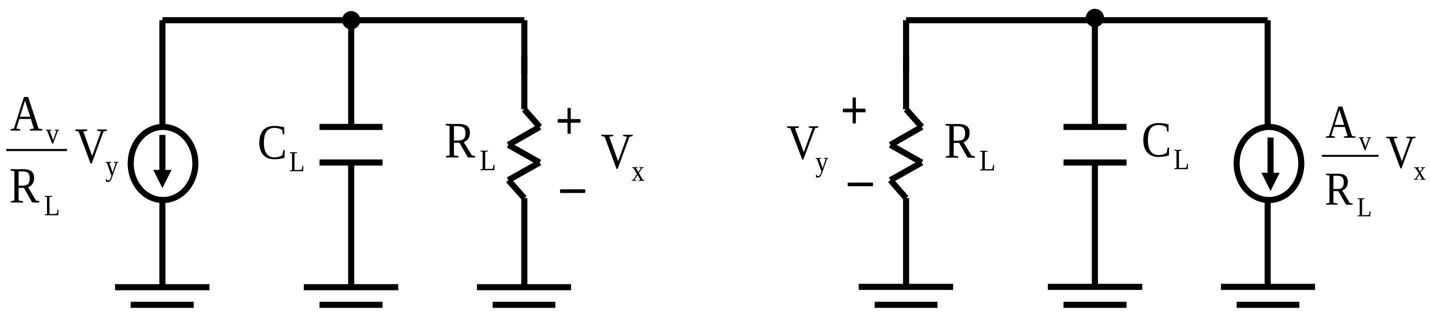
- Hysteresis due to
  - Circuit condition is not memoryless
    eg. If a comparator toggles in one direction, it might have a tendency to stay in that direction.
    - In order to eliminate it, one can reset the different stages before entering track mode.
  - Input-transistor charge trapping
    (will be described later)

Latch-Mode Time Constant

- Simplified model of a track-and-latch stage in its latch phase



- Linearized model
  (low-frequency gain of inverter $A_v = G_m R_L \Rightarrow G_m = \frac{A_v}{R_L}$)



$$\frac{A_V}{R_L} V_y(t) = -C_L[\frac{dV_x(t)}{dt}] - [\frac{V_x(t)}{R_L}]$$

$$\frac{A_V}{R_L} V_x(t) = -C_L[\frac{dV_y(t)}{dt}] - [\frac{V_y(t)}{R_L}]$$

Latch-Mode Time Constant (Cont.)

Let $\tau = R_L C_L$

$$\tau[\frac{dV_x(t)}{dt}] + V_x(t) = -A_v V_y(t) \qquad (1)$$

$$\tau[\frac{dV_y(t)}{dt}] + V_y(t) = -A_v V_x(t) \qquad (2)$$

(2) – (1) $\Rightarrow (\frac{\tau}{A_v - 1})[\frac{dV_o(t)}{dt}] = V_o(t)$

where $V_o(t) = V_x(t) - V_y(t)$ is the voltage difference between the output voltages of the inverters

$$\Rightarrow V_o(t) = V_o(0)e^{(A_v - 1)t/\tau}$$

where $V_o(0)$ is the initial voltage difference at the beginning of the latch phase

$$\Rightarrow \tau_{latch} = \frac{\tau}{A_V - 1} \cong \frac{R_L C_L}{A_V} = \frac{C_L}{G_m}$$

Latch-Mode Time Constant (Cont.)

$$\begin{cases} C_L = K_1 WLC_{ox} & ; \quad K_1 = 1 \sim 2 \\ G_m = K_2 g_m = K_2 \mu_n C_{ox} \dfrac{W}{L} V_{eff} & ; \quad K_2 = 1.5 \sim 2 \end{cases}$$

$$\Rightarrow \tau_{latch} = \frac{K_1}{K_2} \frac{L^2}{\mu_n V_{eff}}$$

$\Rightarrow \tau_{latch}$ depends primarily on the technology

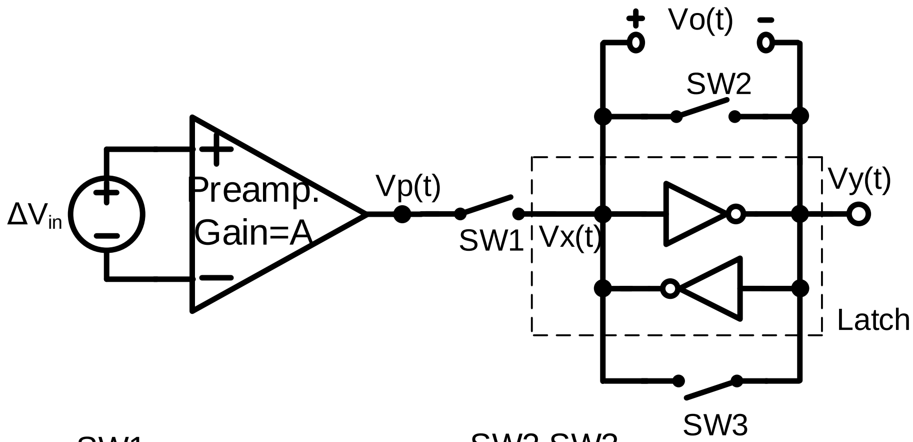
- For a voltage difference of ΔV_{logic} to be obtained in order for succeeding logic circuitry to safely recognize the correct output value

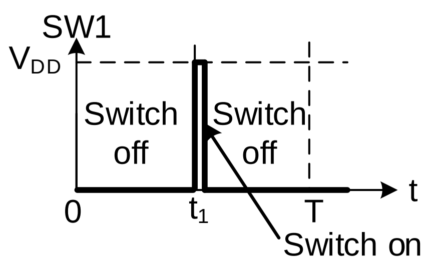
$$T_{latch} = \frac{C_L}{G_m} \ln\left(\frac{\Delta V_{logic}}{V_o(0)}\right) = K_3 \frac{L^2}{\mu_n V_{eff}} \ln\left(\frac{\Delta V_{logic}}{V_o(0)}\right)$$

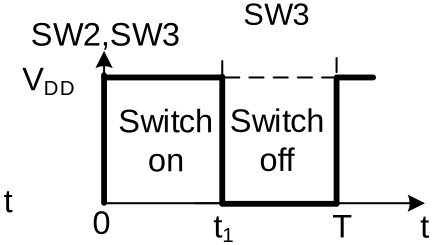
- If $\Delta V_o(0)$ is small, this latch time can be large, perhaps larger than the allowed time for the latch phase. Such an occurrence is often referred to as metastability.

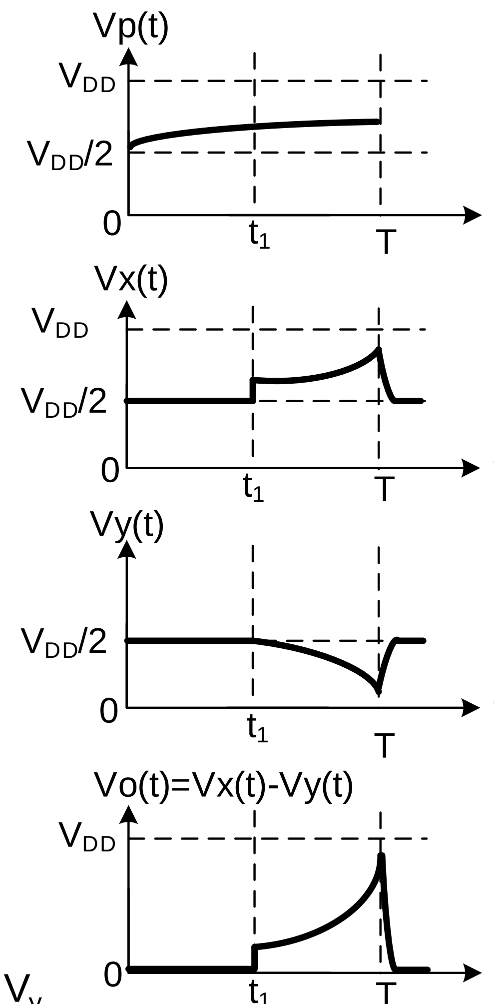
Example of CMOS and BiCMOS Comparators

- Example-1:
  - A comparator that has a preamplifier and a positive-feedback latch







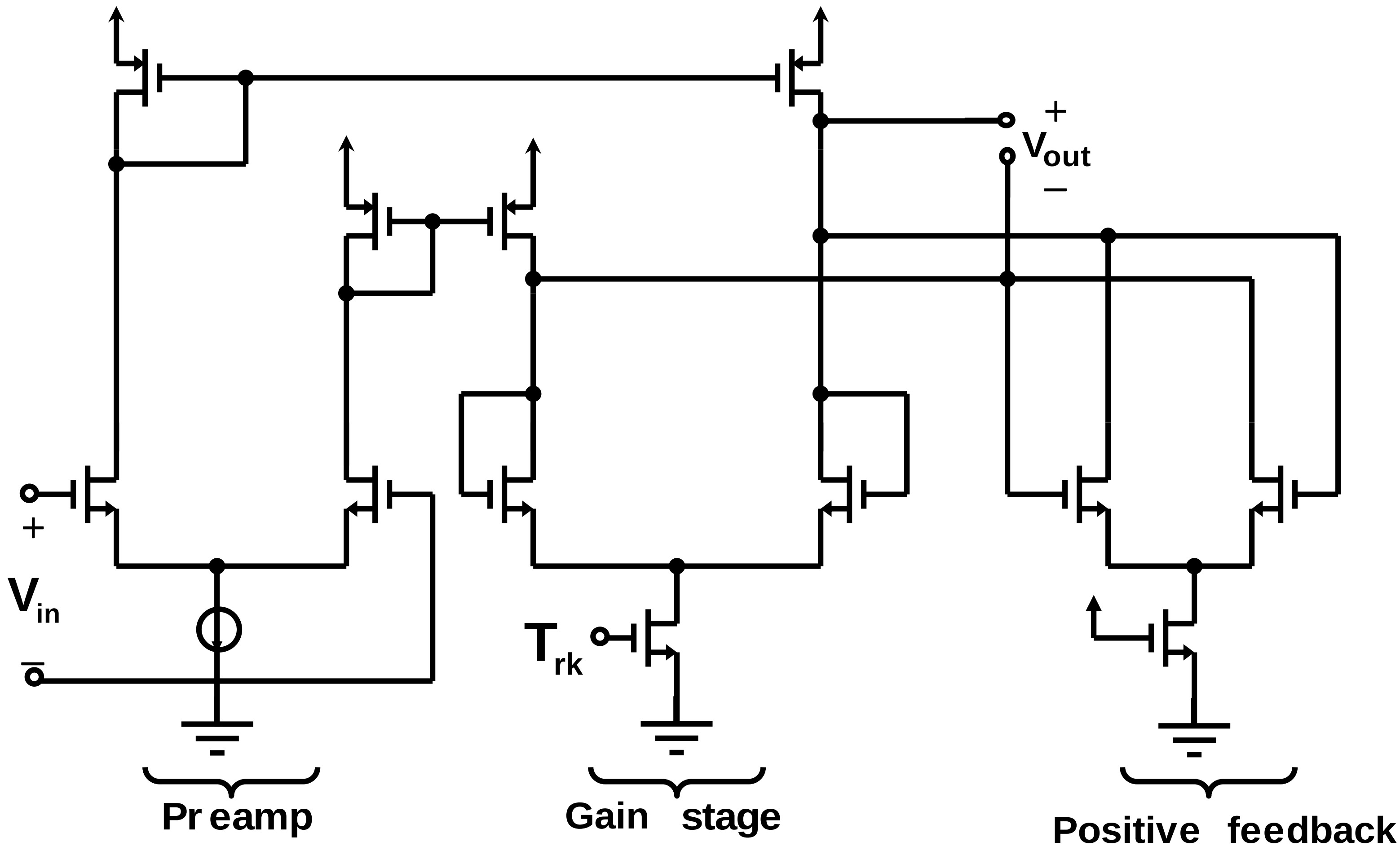


$$V_x(t) - V_y(t) = \underbrace{[A \times \Delta V_{in}(1 - e^{-t_1/\tau})]}_{\text{Pre-amplifying}} \times \underbrace{e^{\frac{t-t_1}{\left(R_L C_L / (A_v - 1)\right)}}}_{\text{Latching}}$$

where A_v, C_L and R_L are the inverter gain, total capacitance of each node V_x and V_y, and total resistance of each node V_x and V_y

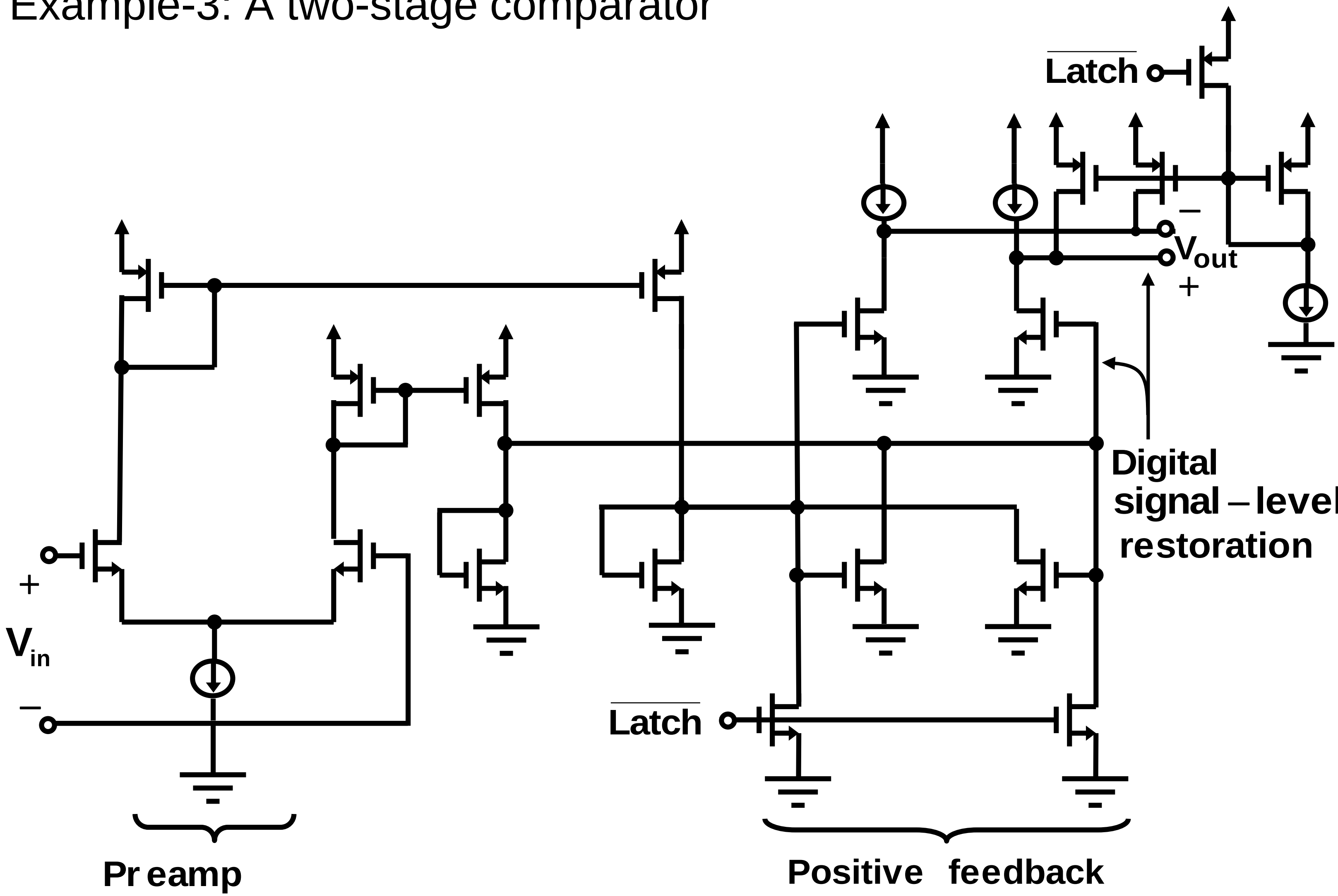
Examples of CMOS and BiCMOS Comparators (Cont.)

- Example-2:
  - A two-stage comparator that has a preamplifier and a positive-feedback track-and-latch stage



Examples of CMOS and BiCMOS Comparators (Cont.)

- Example-3: A two-stage comparator



Input Transistor Charge Trapping

- When n-channel transistors are stressed with large positive gate voltages, electrons can become trapped via a tunneling mechanism in which electrons tunnel to oxide traps. During the time they are trapped, the effective transistor threshold voltage is increased. This leads to a comparator hysteresis on the order of 0.1 to 1mV.

- The time constant for the release of these trapped electrons is on the order of milliseconds and is much longer than the time it takes for them to become trapped.

- This effect correlates well with transistor 1/f noise and is much smaller in p-channel transistors.
  - P-channel transistor exhibit much less hysteresis than n-channel transistors.

Input Transistor Charge Trapping (Cont.)

- One approach of minimizing this effect is to flush the input transistors after each use where the junctions and wells of n-channel transistors are connected to a positive power supply whereas the gates are connected to a negative power supply. This effectively eliminates the trapped electrons.

- Alternately, two input stages can be used for the comparator– a rough stage can be used during times when large signals with overloads are possible, whereas a fine stage can be used during times when accurate comparisons are necessary and it can be guaranteed that no large signals are present.